REMARKS

Claims 1-8 and 10-19 are pending in this application. Claims 1-2, 4-7, 12-14 and 17-19 are amended, and claims 9 and 20 have been canceled herein. No new matter has been added. Applicants respectfully request reconsideration of the claims in view of the following remarks.

The drawings have been objected to because descriptive labels are needed for Figures 1-5. In response, replacement drawings have been provided herewith that include descriptive labels.

Claim 4 has been objected to for failing to include indents. This claim has been rewritten to include indents. Claim 20 has been canceled so that any objection to this claim is now moot.

Claims 1-20 have been rejected under 35 U.S.C. § 112, second paragraph. Applicant respectfully submits that the claims, as amended, fully meet the requirements of Section 112. In particular, each of the issues raised by the Office Action are addressed by the above amendments.

The present application claims priority to a German application and thus was derived from a translation of the priority document. With respect to the term "useful data," the German parent application uses the term "Nutzdaten," which can more clearly be translated to "user data" or "utility data." To avoid any confusion, the claims have been amended to simply use the term "data." Further, the term "memory checking device" has been amended to "memory control device," which is derived from the German term "Speicherkontrolleinrichtungen."

Claims 1, 12 and 17 have been rejected under 35 U.S.C. § 102(e) as being anticipated by Yoshimura (U.S. Patent No. 6,421,274, hereinafter "Yoshimura"). No other claims have been rejected in view of prior art. Applicants respectfully traverse this rejection.

Claims 1, 12 and 17 have been amended to include the feature of original claim 9, which was not rejected in view of prior art.

In particular, claim 1 now refers to a memory module comprising a plurality of DRAMs and a combined buffer and error checking module. The memory module according toYoshimura, on the other hand, is a nonvolatile semiconductor memory device.

Applicant notes that the nonvolatile semiconductor memory device according to Yoshimura comprises two buffer RAMS. First, there is no indication that the buffer RAMS are DRAMs. Also, the buffer RAMS are provided between the flash memory of the memory device and a host interface. According to the invention a buffer device is connected to the DRAM devices, whereas according to Yoshimura the RAM is the buffer.

According to claim 12, the buffer/retriever is operable to condition data signals that are transferred to memory modules, which in each case comprise a plurality of DRAM devices. The memory device of Yoshimura does not comprise a buffer/retriever that is operable to condition data signals that are transferred to memory modules that comprise a plurality of DRAM devices, as Yoshimura does not refer to DRAMs at all.

Similarly, claim 17 requires "storing the data in the DRAM devices; . . . [and] forming in the buffer and error checking module, during a transfer of stored data from the DRAM devices to a memory control device of the data memory system, a corresponding set of check data." Yoshimura does not teach or suggest the limitations of claim 17.

Applicant has made a diligent effort to place the claims in condition for allowance. However, should there remain unresolved issues that require adverse action, it is respectfully requested that the Examiner telephone Ira S. Matsil, Applicant's attorney, at 972-732-1001 so that such issues may be resolved as expeditiously as possible. No fee is believed due in

connection with this filing. However, should one be deemed due, the Commissioner is hereby authorized to charge Deposit Account No. 50-1065.

Respectfully submitted,

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Date

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